What Is Claimed Is:

1. An ESD protection component, comprising:

at least two MOS field effect transistors (FETs) of a first conductivity type, having two gates and formed in parallel on a first semiconductive layer having a second conductivity type;

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

a first doping area of the second conductivity type, formed in the connecting area.

2. The ESD protection component in claim 1, wherein the ESD protection component further comprises a guard ring of the second conductivity type.

3. The ESD protection circuit in claim 2, wherein the first conductive layer is connected to a power supply through the guarding ring.

4. The ESD protection circuit in claim 1, wherein the first well is separated from the drains of the MOS FETs.

5. The ESD protection circuit in claim 1, wherein each of the MOS FETs has a source region of the first conductivity type, coupled to a power rail.

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6. The ESD protection circuit in claim 1, wherein the first well is coupled to a pad through the extension areas.

7. The ESD protection circuit in claim 1, wherein the first doping region is coupled to a pad.

8. The ESD protection circuit in claim 1, wherein each of the MOS FETs has a drain region of the first conductivity type coupled to a pad.

9. An ESD protection component, comprising:

at least two MOS field effect transistors (FETs) of a first conductivity type, comprising:

two gates, formed in parallel on a first semiconductive layer having a second conductivity type;

two sources of the first conductivity type, coupled to a power supply; and

two drains of the first conductivity type;

a first well having a first conductivity type, formed on the first semiconductive layer, comprising:

a connecting area, formed between the MOS FETs;

Two parallel extension areas, formed perpendicular to the gates of the MOS FETs; and

a first doping area of the second conductivity type, formed in the connecting area, and coupled to a pad; and

a guard ring of the second conductivity type, formed on the first semiconductive layer, coupled to the power supply;

wherein the firsPt well is coupled to the pad through the extension areas.